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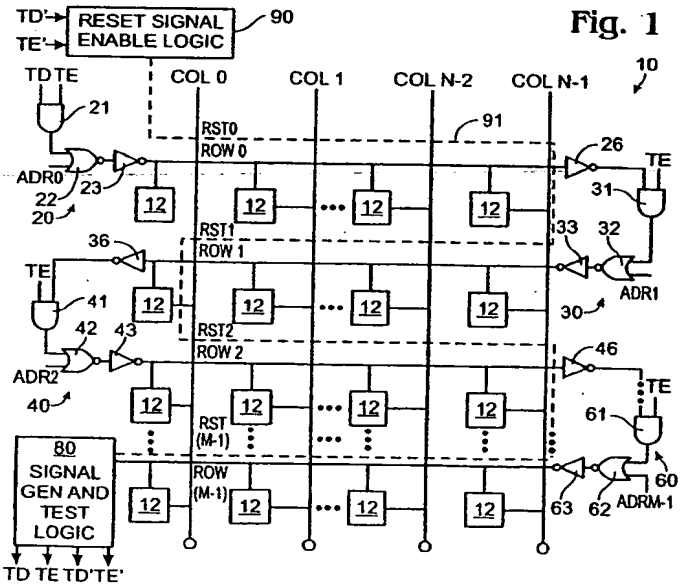
(54) Active pixel sensor circuit

(57) An active pixel sensor (APS) circuit (10) which provides enhanced test and signal processing capabilities. APSs usually include pixel cells (12, 112) arranged in an array of rows and columns. Selectively enableable coupling conductors (30, 40, 60, 230, 240) are provided between principal conductors in the array to permit a signal on one principal conductors to propagate to another principal conductors. The principal conductors include row, reset and column conductors. Signal propagation for testing purposes and for normal mode operation is improved.

Fig. 1



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test and operation is shown. The sensor is preferably formed as matrix 10 that includes a plurality of active pixel cells 12 arranged in M rows and N columns. A pixel cell is provided at the intersection of each row and column. While APSs incorporating this embodiment may be any size, two representative sizes are a 2M pixel APS that is 1280x1600 and a 1.3M pixel APS that is 1024x1280. Each pixel preferably has dimensions of less than 5 μm x 5 μm.

[0014] Figures 1 and 3-4 illustrate an embodiment of serpentine or like signal propagation scheme. Features of the serpentine or like connection scheme can be used during test mode or normal mode operation. Test mode operation will be discussed first followed by normal mode operation.

Test Mode

[0015] One embodiment provides selectably continuous signal conductors that incorporate the row signal conductors and the reset signal conductors. A similar arrangement is preferably provided for the column signal conductors. These arrangements test the metal integrity of the row, reset and column signal conductors, respectively. The tests preferably entail assertion of a test signal onto the first of the row, reset or column conductors. The test signal is propagated through the remainder of the conductors (of that type) and read as an output of the last conductor. Receipt of the correct test signal at the output indicates metal integrity for the type of conductor (row, reset or column) under test. The manner in which these tests are implemented is now discussed in more detail.

[0016] For row conductors, an initial test signal is preferably delivered to row0 select logic 20 that includes an AND gate 21, NOR gate 22 and inverter 23. AND gate 21 receives a test enable (TE) signal and a test data (TD) signal. The TD signal is passed through AND gate 21 to NOR gate 22. The other input of NOR gate 22 is the row0 address signal which is held low during test mode. The TD signal continues through inverter 26 to row1 select logic 30. AND gate 31 and NOR gate 32 provide the same functions as their counterparts in row0 select logic 20. NOR gate 32 passes the TD signal onto row1 through inverter 33.

[0017] The TD signal on row1 is then propagated through inverter 36 to row2 select logic 40 which includes an AND gate 41, NOR gate 42 and inverter 43. Row2 select logic 40 passes the TD signal onto row2. This serpentine pattern that propagates the TD signal back and forth down the even and odd rows, respectively, is preferably repeated until the last row(M-1) is reached. Row(M-1) select logic 60 preferably includes an AND gate 61, NOR gate 62 and inverter 63. Similar to the other row select circuit, row(M-1) select logic passes the test signal onto row(M-1).

[0018] The TE signal is preferably generated by the test signal generation and comparison logic (signal gen and test logic) 80 and delivered to each of the row select logic circuits (and counter part reset select logic circuits discussed below). The TE signal enables test mode operation. The TD signal preferably provides both logic high and logic low signals and may include serial data of different logic states. In one test, data is input to row0 select logic 20 and compared to that received from row (M-1) by test logic 80.

[0019] The row signal conductors (and the serpentine connector traces at each end) have line widths of approximately 0.5um and these lines have a parasitic capacitance and resistance associated therewith. These parasitics produce an inherent delay. The logic components also induce delay, but this delay tends to be significantly less (e.g., a few hundred picoseconds) than that contributed by the signal trace dimensions. The delay induced by a row conductor in the APS of Fig. 1, assuming 1,600 columns, is approximately 5ns. For an APS of 1280 rows this achieves a signal propagation time from top to bottom of 6.4 μs.

[0020] Fig. 1 also shows a serpentine reset line 91 arrangement. The arrangement is shown in dash lines to distinguish it from the row lines and also so as to not crowd the drawing. It is to be understood that the same logic and signal conductors provided for row conductor test are preferably provided for reset conductor test (and for normal mode reset operation). Thus, reset select logic between each row includes an AND gate, NOR gate and inverter (and test enable and individual address signals, etc.). The test logic 80 provides a separate test enable and test data signal for the reset conductors. These signals are designated TE' and TD' respectively.

[0021] In a preferred test mode, the test of row signal conductors and reset signal conductors are carried out simultaneously. The TD and TD' signal, however, are preferably the complement of each other to increase the likelihood of detecting shorts or open circuits, e.g., bridging, etc.

[0022] Referring to Fig. 2, a schematic diagram of a representative active pixel cell for use in accordance with the present invention is shown. Cell 12 preferably includes three transistors 13-15 (which are typically n-type field-effect transistors) and a light sensitive or "photo" diode 11. Transistors 13 and 14 are coupled to V_{DD} and transistor 15 is coupled to the source of transistor 14. A reset signal is applied to the gate of transistor 13 and a row select signal is applied to the gate of transistor 15.

[0023] In a typical mode of operation, the reset line is asserted high to charge the parasitic capacitance of the reversed biased photo diode to a reset level. After diode output node 17 has stabilized, the reset is pulled low, allowing photo induced charge carriers to discharge the photo diode at a rate proportional to the incident light intensity. After a specific exposure time, the row select line is asserted high allowing the voltage at node 17 to be sampled at the cell output node 19 (where

bal (i.e., simultaneous) reset signal to all cells generate an unacceptable EMI current spike (as discussed above).

[0040] Reset signal enable logic 90 achieves assertion of a reset signal, for the start of imaging data integration, that propagates through the reset conductors as discussed above, experiencing approximately 5 ns of delay per individual reset conductor (i.e., per row) and delivering the reset signal to all pixel cells in the array (5nsx1280 rows) in 6.4 us.

[0041] This arrangement provides resets in a sufficiently rapid time interval, but does not produce a disadvantageously large amount of EMI (i.e., current spikes, etc.).

[0042] It will be understood that the embodiments disclosed above are capable of further modification, and this specification is intended to cover any variations, uses, or adaptations following, in general, the principles disclosed and including such departures from the present disclosure as come within known or customary practice in the art and as may be applied to the essential features herein before set forth, and as fall within the scope of the appended claims.

[0043] The disclosures in United States patent application no. 09/371,745, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

Claims

1. An active pixel sensor circuit, comprising:

   a substrate;
   a plurality of pixel cells (12, 112) provided on said substrate and arranged in at least a plurality of rows;
   a plurality of first signal conductors (Row0, Row1, Row2) each associated with a given row and coupled to the pixel cells of that row; and
   a plurality of selectably enableable coupling conductors (30, 40, 60, 230, 240), one provided between each of said plurality of first signal conductors, and each providing selectable coupling of the first signal conductor of one row to that of another.

2. The circuit of claim 1, wherein said selectably enableable coupling conductors are provided at alternating ends of said plurality of first signal conductors such that when said coupling conductors are enabled to conduct, a signal input to a first of said first signal conductors propagates in a generally serpentine manner through the remainder of the plurality of first signal conductors.

3. The circuit of claim 1, wherein said selectably enableable coupling conductors are provided at alternating ends of said plurality of first signal conductors such that a signal input to a first of said first signal conductors propagates in a first direction on that first of said first signal conductors, in a second direction on a second of said first signal conductors that is generally opposite of said first direction and in said first direction again on a third of said first signal conductors.

4. The circuit of claims 1, 2 or 3, wherein at least some of said selectably enableable coupling conductors include tri-state logic (30, 40, 60) and a test enable (TE) input, receipt of a correct polarity signal at said test enable input causing a signal on a preceding first signal conductor to be passed through said tri-state logic to a subsequent first signal conductor.

5. The current of any preceding claim, wherein said first signal conductors are one of the group of signal conductors including reset signal conductors and row signal conductors.

6. The circuit of any preceding claim, comprising a plurality of second signal conductors (rst0, rst1, rst2) each associated with a given row and coupled to the pixel cells of that row; and

   a plurality of second selectably enableable coupling conductors, one provided between each of said plurality of second signal conductors, and each providing selectable coupling of the second signal conductor of one row to that of another; and
   wherein said first signal conductors are one of the group of signal conductors including reset signal conductors and row signal conductors, and said second signal conductors are the other of that group.

7. The circuit of any preceding claim, wherein said first signal conductors (30, 40, 60, 230, 240) and said selctably enableable coupling conductors are arranged such that when a signal is input to a first of said first signal conductors and said coupling conductors are enabled, the input signal is sequentially propagated to the remaining first signal conductors in such a manner that a delay is realized before receipt of that input signal at each subsequent one of said first signal conductors; and
   wherein said delay is less than approximately 25 ns per row.

8. The circuit of any preceding claim, wherein said plurality of pixel cells are arranged in a plurality of columns and said circuit includes:

   a plurality of column conductors (col0, col1, colN-2, colN-1) each associated with one of said pixel columns and coupled to the pixel

Fig. 1

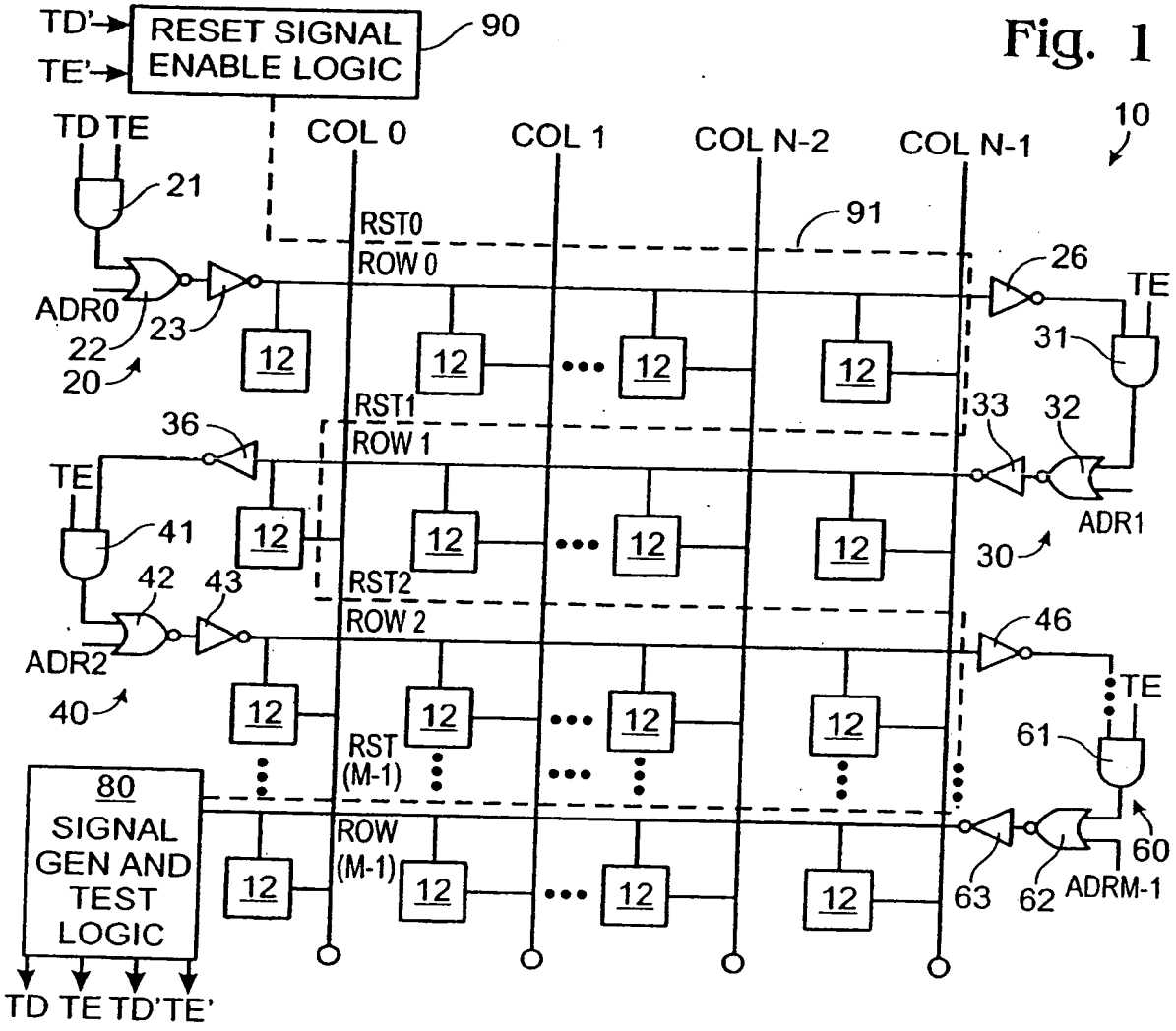
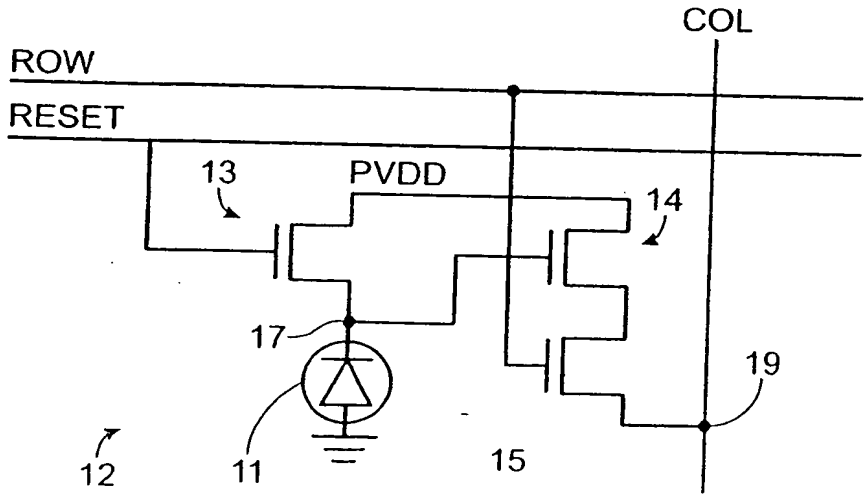


Fig. 2



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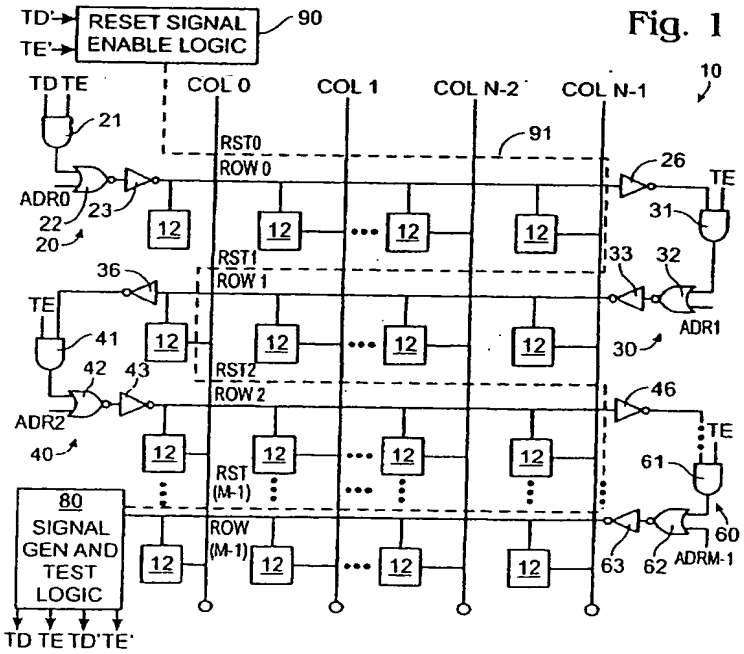

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 30 6302

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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23-01-2002

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